What is claimed is:

1. A method comprising:
preparing a substrate; and
forming one or more dual gate structures in the substrate using only one mask.

2. The method of claim 1, wherein preparing a substrate comprises:
forming a sacrificial oxide layer on a semiconductor.

3. The method of claim 1, wherein preparing a substrate comprises:
forming a gate oxide layer on a semiconductor; and
forming a polysilicon layer on the gate oxide layer.

4. The method of claim 1, wherein forming one or more dual gate structures in the substrate using only one mask comprises:
forming a first gate structure having a first conductivity in the substrate, the first gate structure being formed using one or more blanket implants; and
forming a second gate structure having a second conductivity in the substrate, the second conductivity having a different value than the first conductivity and the second gate structure being formed using only one masking operation.

5. A method comprising:
preparing a substrate;
forming a first gate structure including a PWELL without using a mask; and
forming a second gate structure including an NWELL using only one mask.

6. The method of claim 5, wherein forming a second gate structure including an NWELL using only one mask comprises:
forming a deep NWELL.

7. A method comprising:

preparing a substrate;

forming a first gate structure without using a mask, the gate structure having a NWELL formed in the substrate; and

forming a second gate structure using only one mask, the second gate structure having a PWELL formed in the substrate.

8. The method of claim 7, wherein forming a second gate structure including an PWELL using only one mask comprises:

forming a deep PWELL.

9. A method comprising:

preparing a substrate;

forming a first gate structure including a PWELL having a depth of about 200 nanometers without using a mask; and

forming a second gate structure including an NWELL using only one mask.

10. The method of claim 9, wherein forming a second gate structure including an NWELL using only one mask comprises:

forming a deep NWELL.

11. A method comprising:

preparing a substrate;

forming a first gate structure including an NWELL without using a mask; and

forming a second gate structure using only one mask, the second gate structure including a PWELL having a depth of between about 220 and about 240 nanometers.

12. The method of claim 11, wherein forming a first gate structure including an NWELL without using a mask comprises:

forming a doped polysilicon layer above the NWELL.

13. A method comprising:

preparing a substrate;

forming a first gate structure including a PWELL having a threshold voltage adjust region without using a mask; and

forming a second gate structure including an NWELL using only one mask.

14. The method of claim 13, wherein forming a second gate structure including an NWELL using only one mask comprises:

forming a deep NWELL; and

forming a doped polysilicon layer above the NWELL.

15. A method comprising:

preparing a substrate;

forming a first gate structure without using a mask, the gate structure having a NWELL formed in the substrate; and

forming a second gate structure including a PWELL having a threshold voltage adjust region using only one mask.

16. The method of claim 15, wherein forming a second gate structure including a PWELL having a threshold voltage adjust region using only one mask comprises:

forming a deep PWELL; and

forming a doped polysilicon layer above the PWELL.

17. A method comprising:

preparing a substrate;

forming a first gate structure including only blanket implants; and

forming a second gate structure including an NWELL using only one mask.

18. The method of claim 17, wherein forming a second gate structure including an NWELL using only one mask comprises:

forming an NWELL having a depth of about 200 nanometers.

19. A method comprising:

preparing a substrate;

forming a first gate structure having an NWELL formed using only blanket implants in the substrate; and

forming a second gate structure using only one mask, the second gate structure having a PWELL formed in the substrate.

20. The method of claim 19, wherein forming a second gate structure including an PWELL using only one mask comprises:

forming a deep PWELL.

21. A method of forming one or more dual gate structures, the method comprising:

forming one or more first gate structures by applying at least two blanket implants to a substrate; and

forming one or more second gate structures by applying at least three masked implants to the substrate using only one mask.

22. The method of claim 21, wherein forming one or more first gate structures by applying at least two blanket implants to a substrate comprises:

applying a blanket implant to form one or more wells in the substrate;

applying a blanket implant to form a threshold voltage adjust (V_T) in each of the one or more wells; and

applying a blanket n^+ implant to form an n^+ polysilicon layer in the substrate.

23. The method of claim 21, wherein forming one or more first gate structures by applying at least two blanket implants to a substrate comprises:

applying a blanket implant to form one or more wells in the substrate;

applying a blanket implant to form a threshold voltage adjust (V_T) in each of the one or more wells; and

applying a blanket p^+ implant to form a p^+ polysilicon layer in the substrate.

24. A method of forming one or more dual gate structures, the method comprising:

forming a sacrificial oxide layer on a substrate;

forming a PWELL in the substrate using a blanket implant;

removing the sacrificial oxide layer form the substrate;

forming a gate oxide layer on the substrate;

forming a polysilicon layer on the gate oxide layer;

forming a blanket threshold voltage adjust implant into the PWELL

implanting a dopant into the polysilicon layer; and

forming a gate structure including an NWELL in the substrate using only one mask.

25. The method of claim 24, wherein forming a gate structure including an NWELL in the substrate using only one mask comprises:

masking one or more NWELL regions on the substrate;

forming a deep NWELL in at least one of the one or more NWELL regions;

forming a threshold voltage adjust in the deep NWELL region; and

doping the polysilicon layer above the one or more NWELL regions.

26. A method of forming one or more dual gate structures, the method comprising:

forming a sacrificial oxide layer on a substrate;

forming an NWELL in the substrate using a blanket implant;

removing the sacrificial oxide layer from the substrate;

forming a gate oxide layer on the substrate;

forming a polysilicon layer on the gate oxide layer;

forming a blanket threshold voltage adjust implant into the NWELL

implanting a dopant into the polysilicon layer; and

forming a gate structure including a PWELL in the substrate using only one mask.

27. The method of claim 26, wherein forming a gate structure including an NWELL in the substrate using only one mask comprises:

masking one or more PWELL regions on the substrate;

forming a deep PWELL in at least one of the one or more PWELL regions;

forming a threshold voltage adjust in the deep PWELL region; and

doping the polysilicon layer above the one or more PWELL regions.

28. A method of forming one or more dual gate structures, the method comprising:

forming a sacrificial oxide layer in a substrate;

forming a PWELL in the substrate using a blanket implant;

forming a threshold voltage adjust by a blanket implant into the substrate;

removing the sacrificial oxide layer;

forming a gate oxide layer on the substrate;

implanting a dopant into the polysilicon layer; and

forming a gate structure including an NWELL in the substrate using only one mask.

29. The method of claim 28, wherein forming a gate structure including an NWELL in the substrate using only one mask comprises:

masking one or more NWELL regions in the substrate;

forming an NWELL in at least one of the one or more NWELL regions;

forming a threshold voltage adjust in the deep NWELL region; and

doping the polysilicon layer located above the one or more NWELL regions.

30. A method of forming one or more dual gate structures, the method comprising:

forming a sacrificial oxide layer in a substrate;

forming an NWELL in the substrate using a blanket implant;

forming a threshold voltage adjust by a blanket implant into the substrate;

removing the sacrificial oxide layer;

forming a gate oxide layer on the substrate;

implanting a dopant into the polysilicon layer; and

forming a gate structure including a PWELL in the substrate using only one mask.

31. The method of claim 30, wherein forming a gate structure including a PWELL in the substrate using only one mask comprises:

masking one or more PWELL regions on the substrate;

forming a deep PWELL in at least one of the one or more PWELL regions;

forming a threshold voltage adjust in the deep PWELL region; and

doping the polysilicon layer above the one or more PWELL regions.

32. A method of forming one or more dual gate structures, the method comprising:

forming a gate oxide layer on the substrate;

forming a polysilicon layer on the gate oxide layer;

forming a PWELL using a blanket PWELL implant;

forming a blanket threshold voltage adjust;

doping the polysilicon layer using a blanket implant; and

forming a gate structure including an NWELL in the substrate using only one mask.

33. The method of claim 32, wherein forming a gate structure including an NWELL in the substrate using only one mask comprises:

masking one or more NWELL regions on the substrate;

forming an NWELL in at least one of the one or more NWELL regions;

forming a threshold voltage adjust in the NWELL region; and

doping the polysilicon layer above the one or more NWELL regions.

34. A method of forming one or more dual gate structures, the method comprising:

forming a gate oxide layer on the substrate;

forming a polysilicon layer on the gate oxide layer;
forming an NWELL using a blanket NWELL implant;
forming a blanket threshold voltage adjust;
doping the polysilicon layer using a blanket implant; and
forming a gate structure including a PWELL in the substrate using only one mask.

35. The method of claim 34, wherein forming a gate structure including a PWELL in the substrate using only one mask comprises:
masking one or more PWELL regions on the substrate;
forming a deep PWELL in at least one of the one or more PWELL regions;
forming a threshold voltage adjust in the deep PWELL region; and
doping the polysilicon layer above the one or more PWELL regions.

36. A method of forming one or more dual gate structures, the method comprising:
forming one or more gate structures including a PWELL without a mask;
masking one or more NWELL regions; and
forming one or more gate structures including an NWELL in at least one of the one or more NWELL regions.

37. A method of forming one or more dual gate structures, the method comprising:
forming one or more gate structures including an NWELL without a mask;
masking one or more PWELL regions; and
forming one or more gate structures including a PWELL in at least one of the one or more PWELL regions.

38. A method of forming one or more dual gate structures, the method comprising:
forming one or more gate structures including a PWELL using blanket implants;
masking one or more NWELL regions; and
forming one or more gate structures including an NWELL in at least one of the one or more NWELL regions.

39. A method of forming one or more dual gate structures, the method comprising:

forming one or more gate structures including an NWELL using blanket implants;

masking one or more PWELL regions; and

forming one or more gate structures including a PWELL in at least one of the one or more PWELL regions.

40. A method comprising:

forming one or more PWELL gate structures by applying at least three blanket implants to a substrate;

masking the substrate only once to define a number of masked implant areas; and

forming one or more NWELL gate structures by applying one or more masked implants in the one or more masked implant areas.

41. A method comprising:

forming one or more NWELL gate structures by applying at least three blanket implants to a substrate;

masking the substrate only once to define a number of masked implant areas; and

forming one or more PWELL gate structures by applying one or more masked implants in the one or more masked implant areas.

42. A method comprising:

forming one or more PWELL gate structures in a substrate without using a mask; and

forming one or more NWELL gate structures in the substrate using one mask.

43. A method comprising:

forming one or more NWELL gate structures in a substrate without using a mask; and

forming one or more PWELL gate structures in the substrate using one mask.

44. A method comprising:

forming one or more NWELL gate structures in a substrate; and

forming one or more PWELL gate structures in the substrate using a plurality of implant operations and one mask.